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## Q-modules: internally clocked delay-insensitive modules

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### Abstract

Q-modules are internally clocked modules that can be used to satisfy delay-insensitive sp delay element is required with a one-sided bound that its value be greater than the maxim combination logic. Prototypes of components to implement Q-modules have been designe program, QSYN, to place instances of these components, personalize a PLA, and genera file for a CMOS realization, including the delay circuitry, is being developed. Testability is advantages of Q-modules over clock-free delay-insensitive modules; circuitry is included i the logic and interconnections

### Index Terms

Inspec

#### Controlled Indexing

[CMOS integrated circuits](#) [asynchronous sequential logic](#) [integrated logic circuit: design](#) [logic testing](#) [sequential circuits](#)

#### Non-controlled Indexing

[CMOS realization](#) [Q-modules](#) [QSYN](#) [delay-insensitive](#) [internally clocked](#) [te testing](#)

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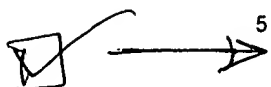
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